

FIG. 1A

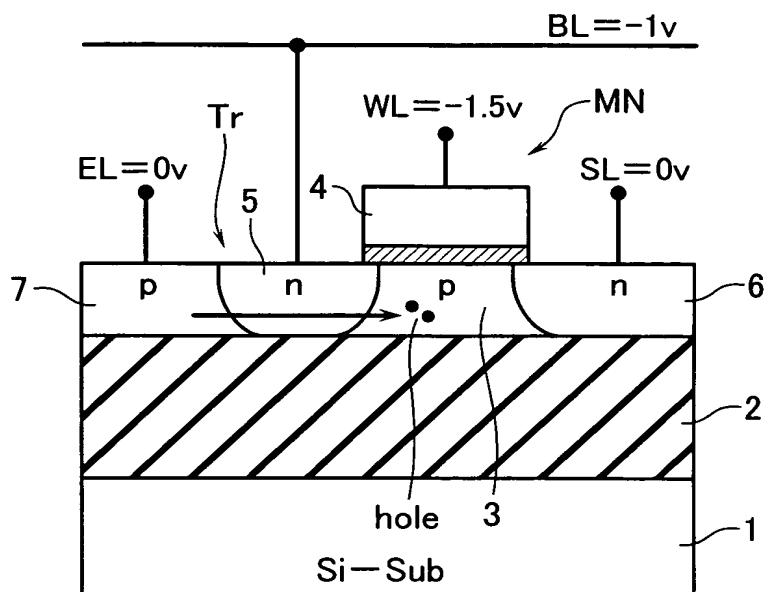


FIG. 1B

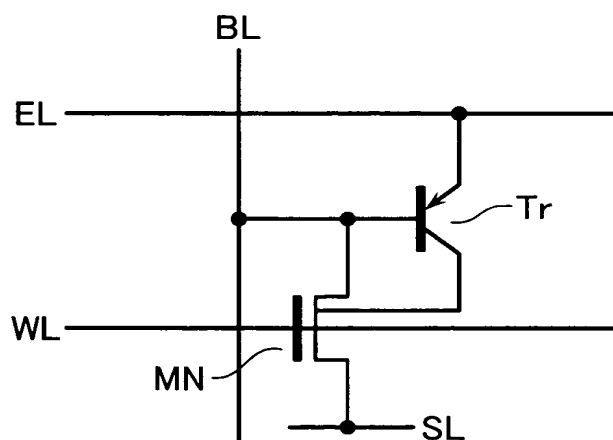


FIG. 2

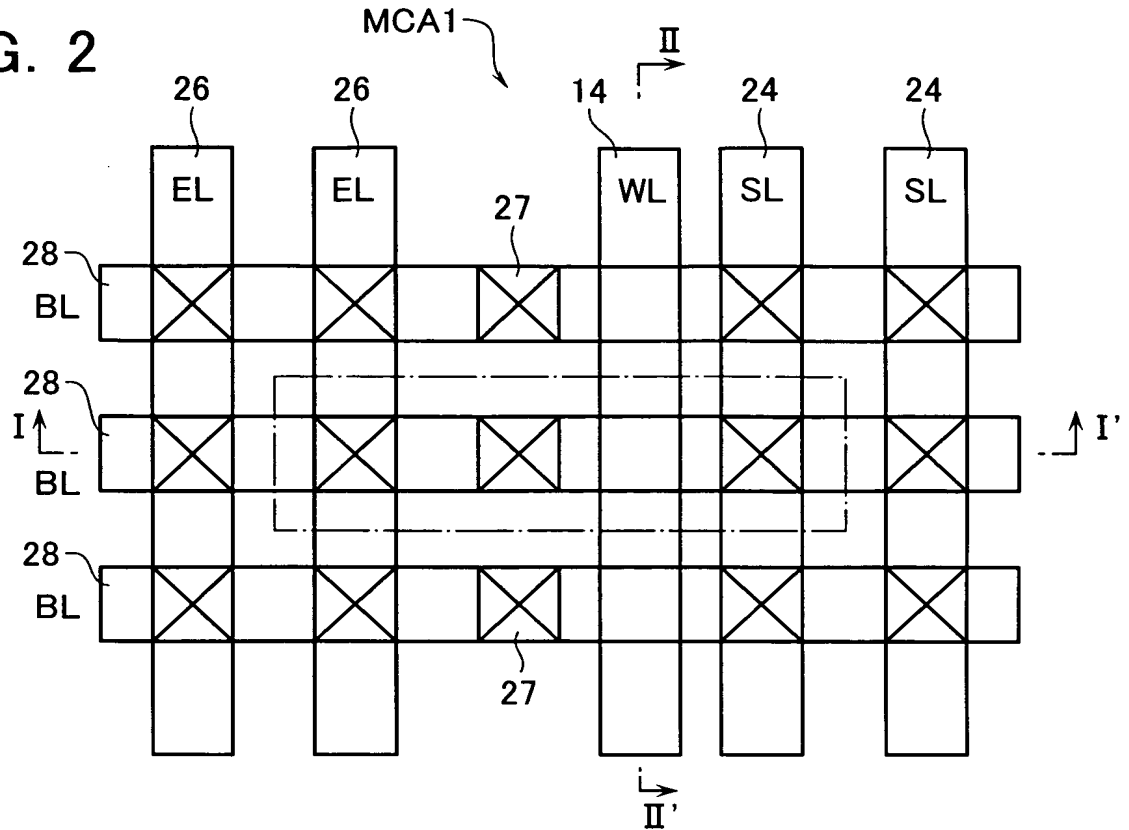


FIG. 3

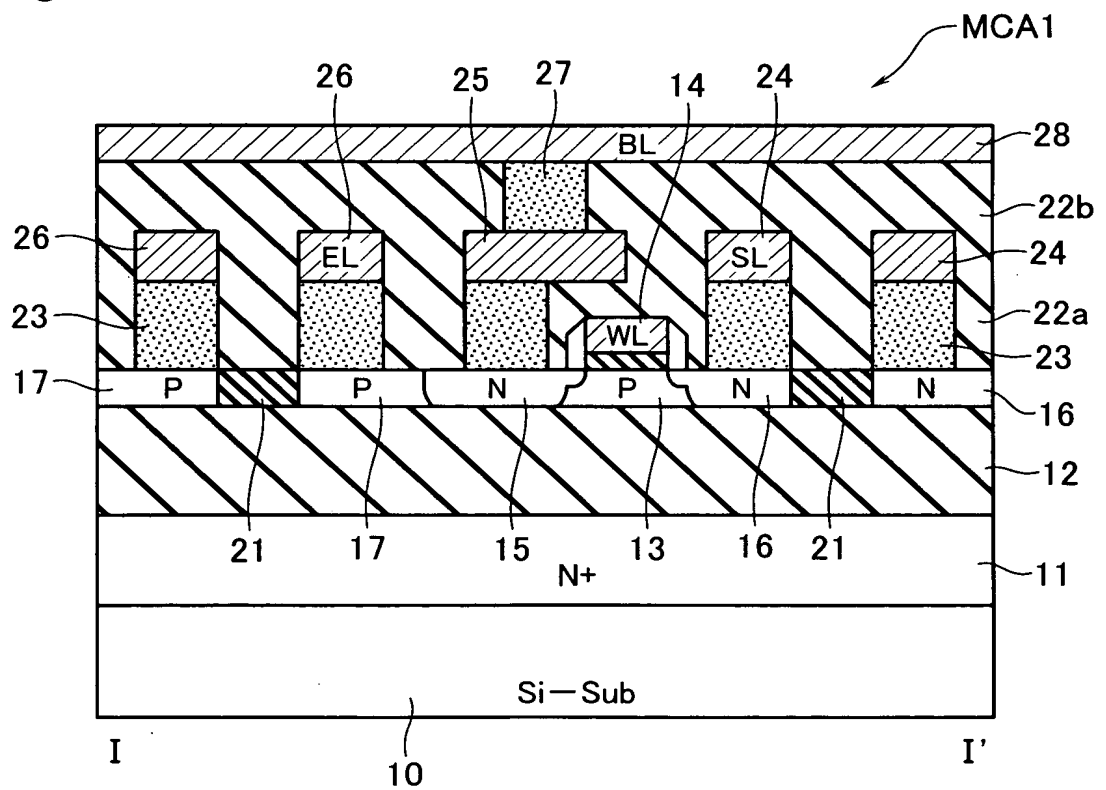


FIG. 4

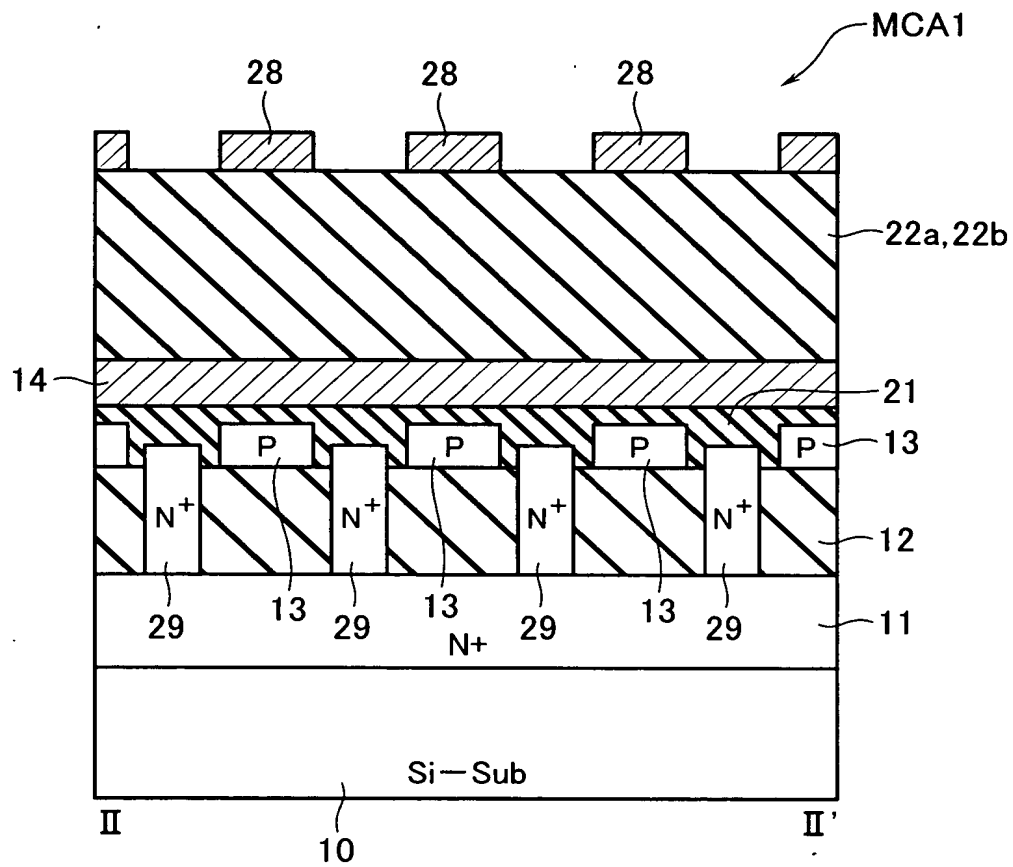


FIG. 5

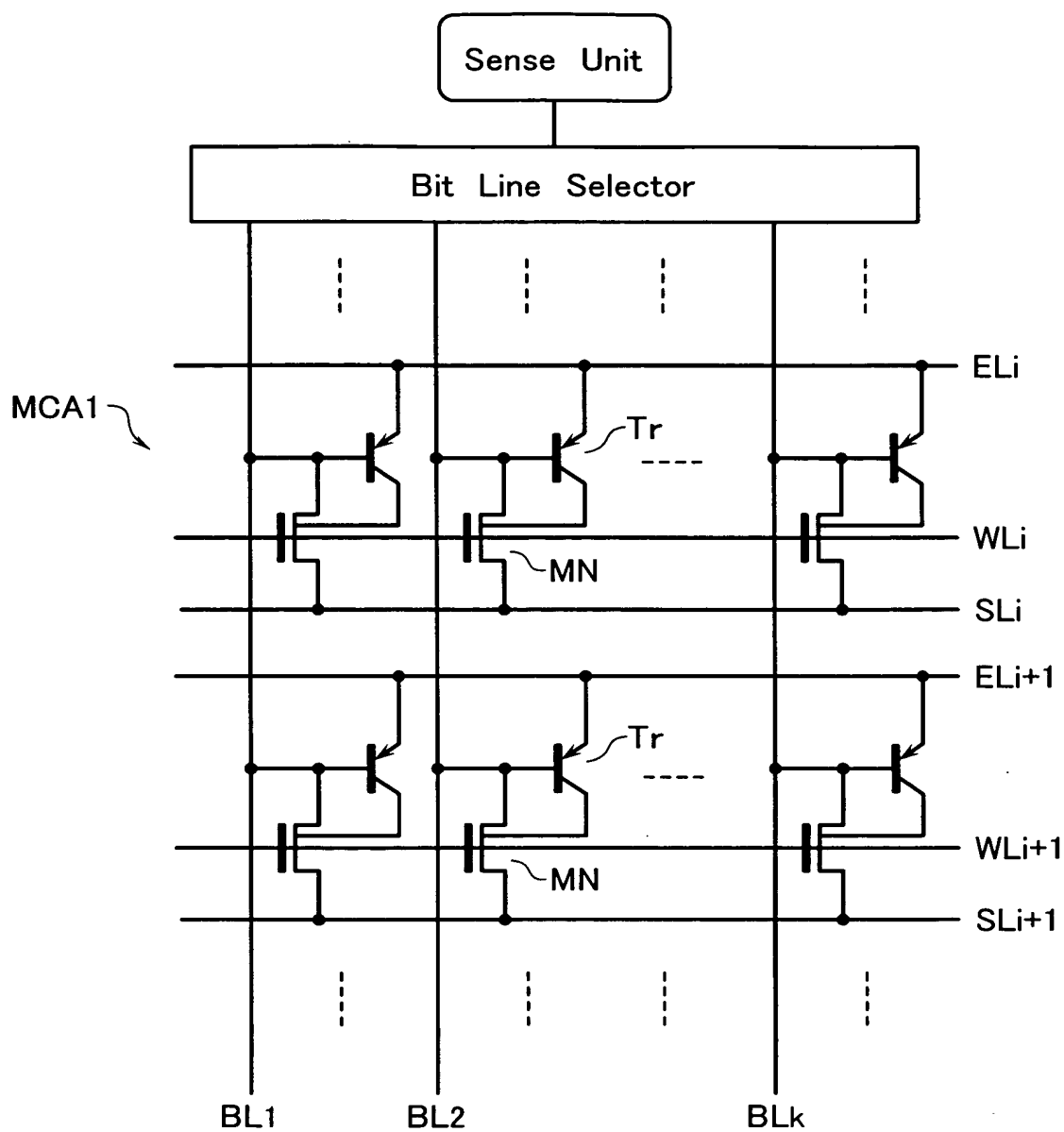


FIG. 6

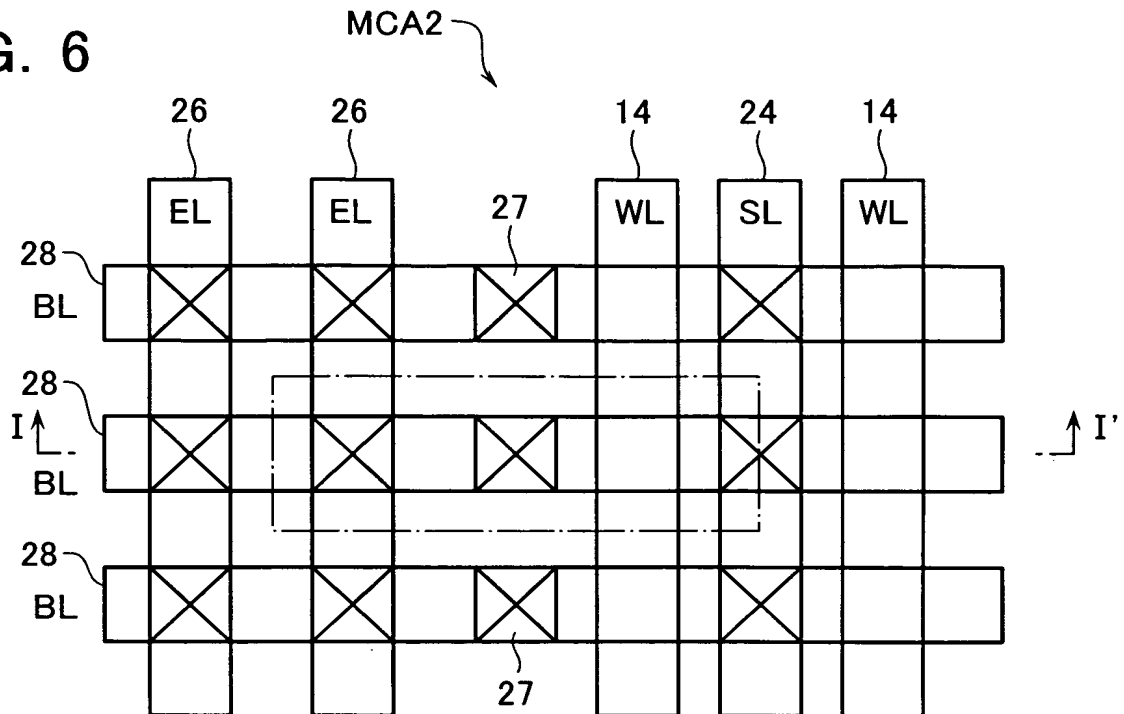


FIG. 7

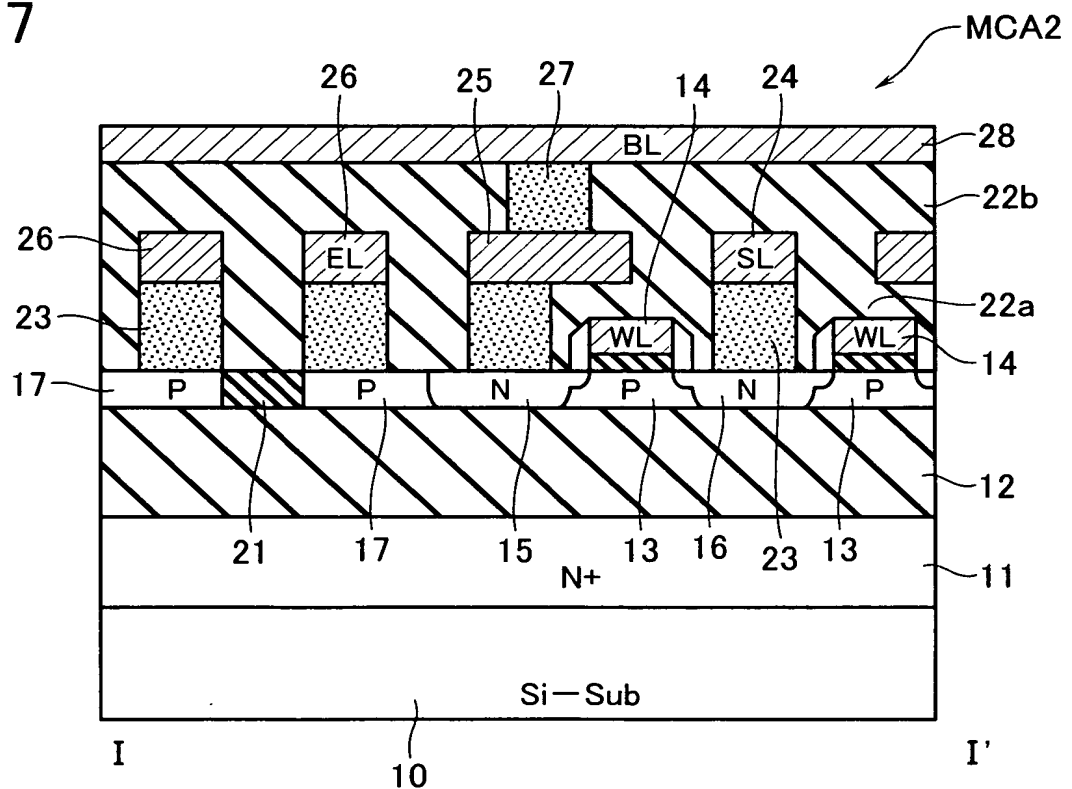


FIG. 8

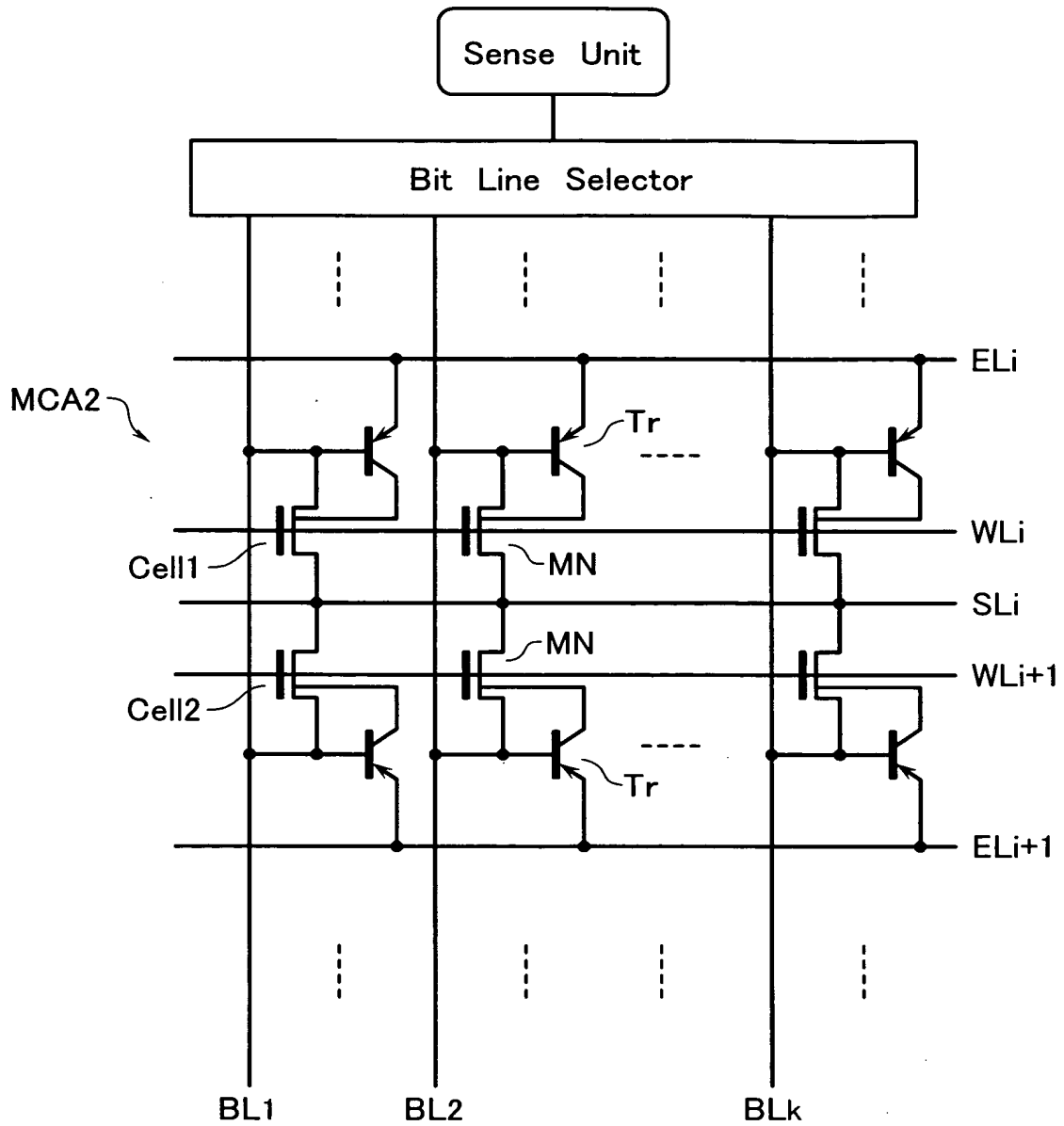


FIG. 9

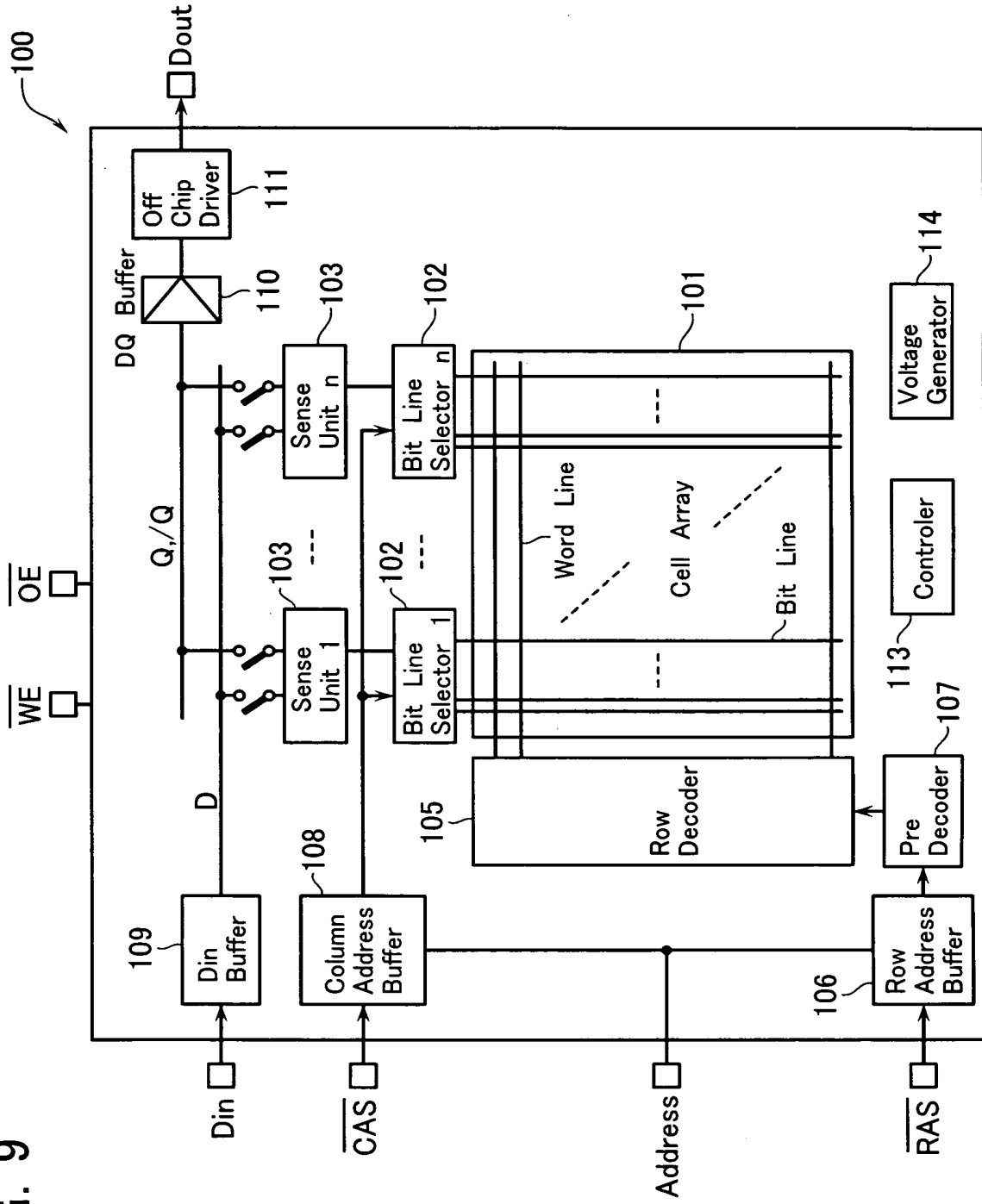


FIG. 10

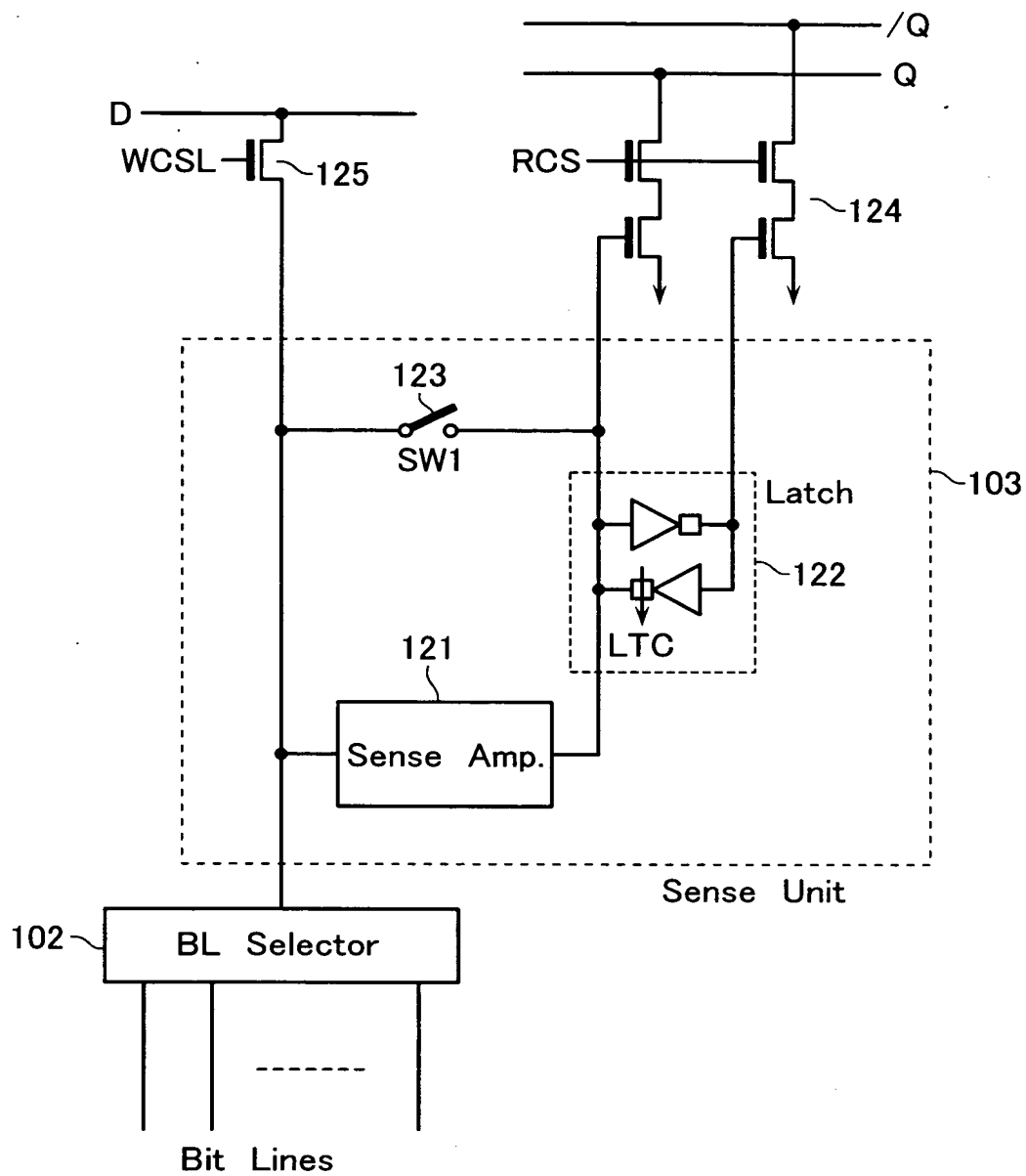


FIG. 11

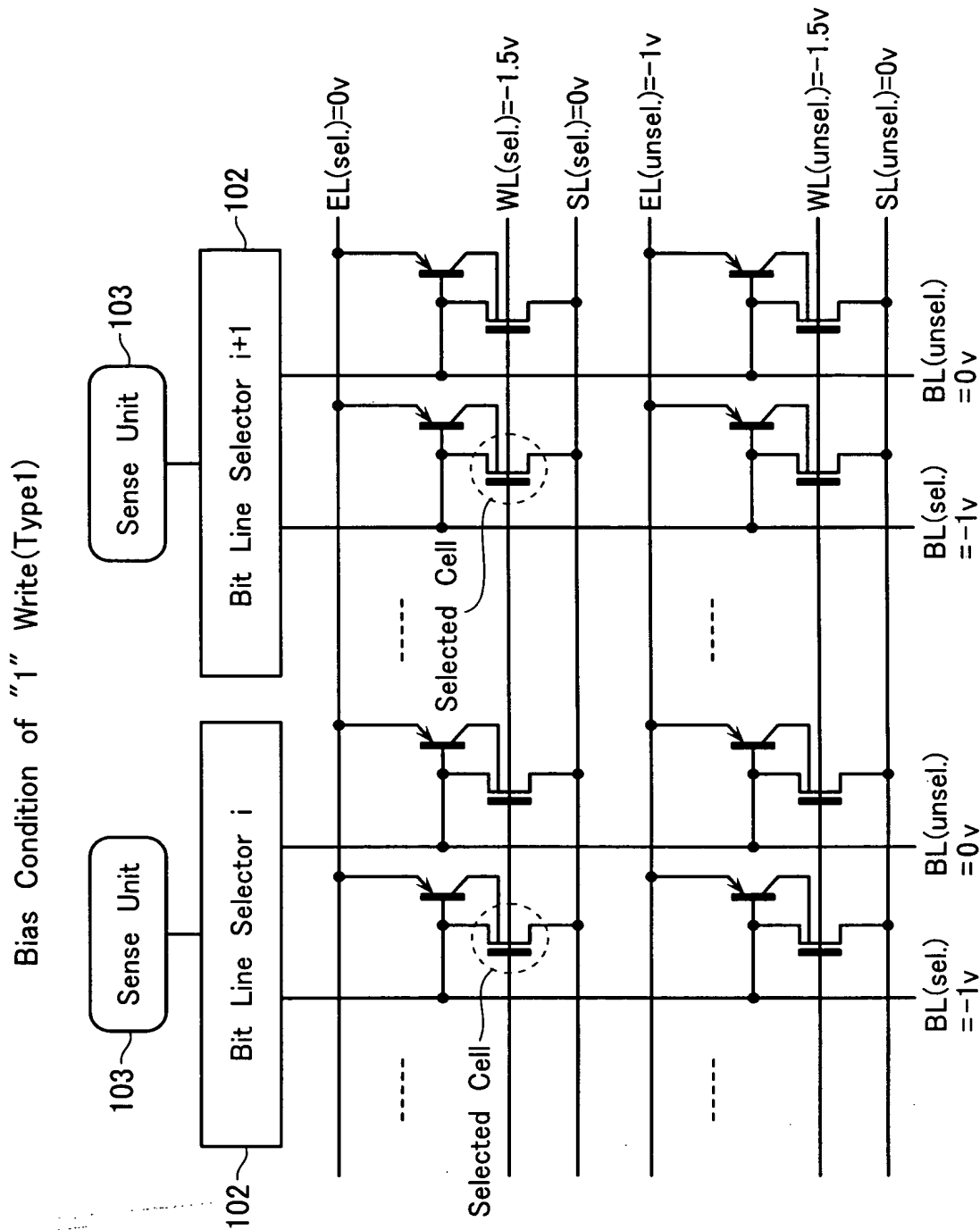


FIG. 12

Bias Condition of "0" Write

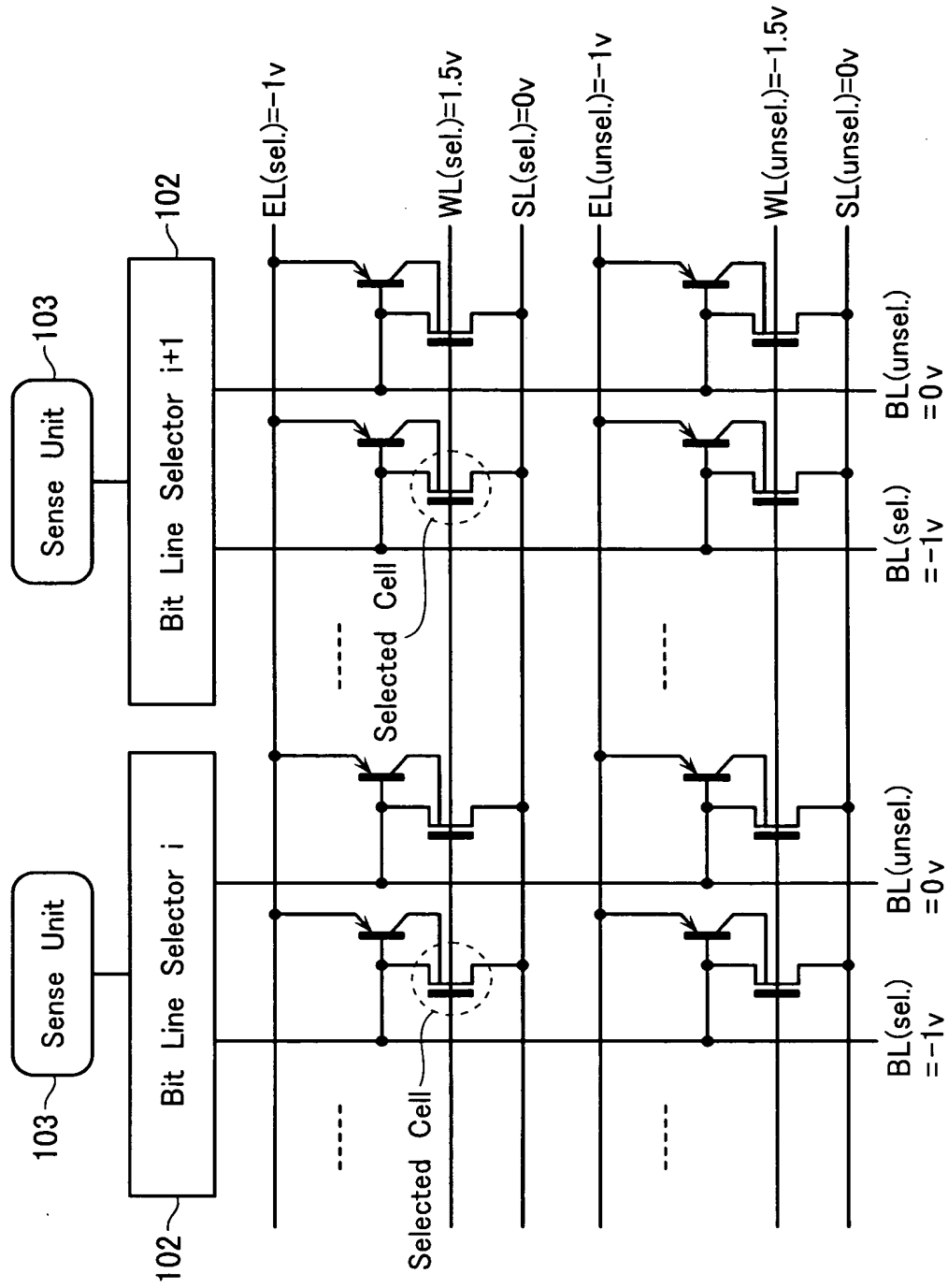


FIG. 13

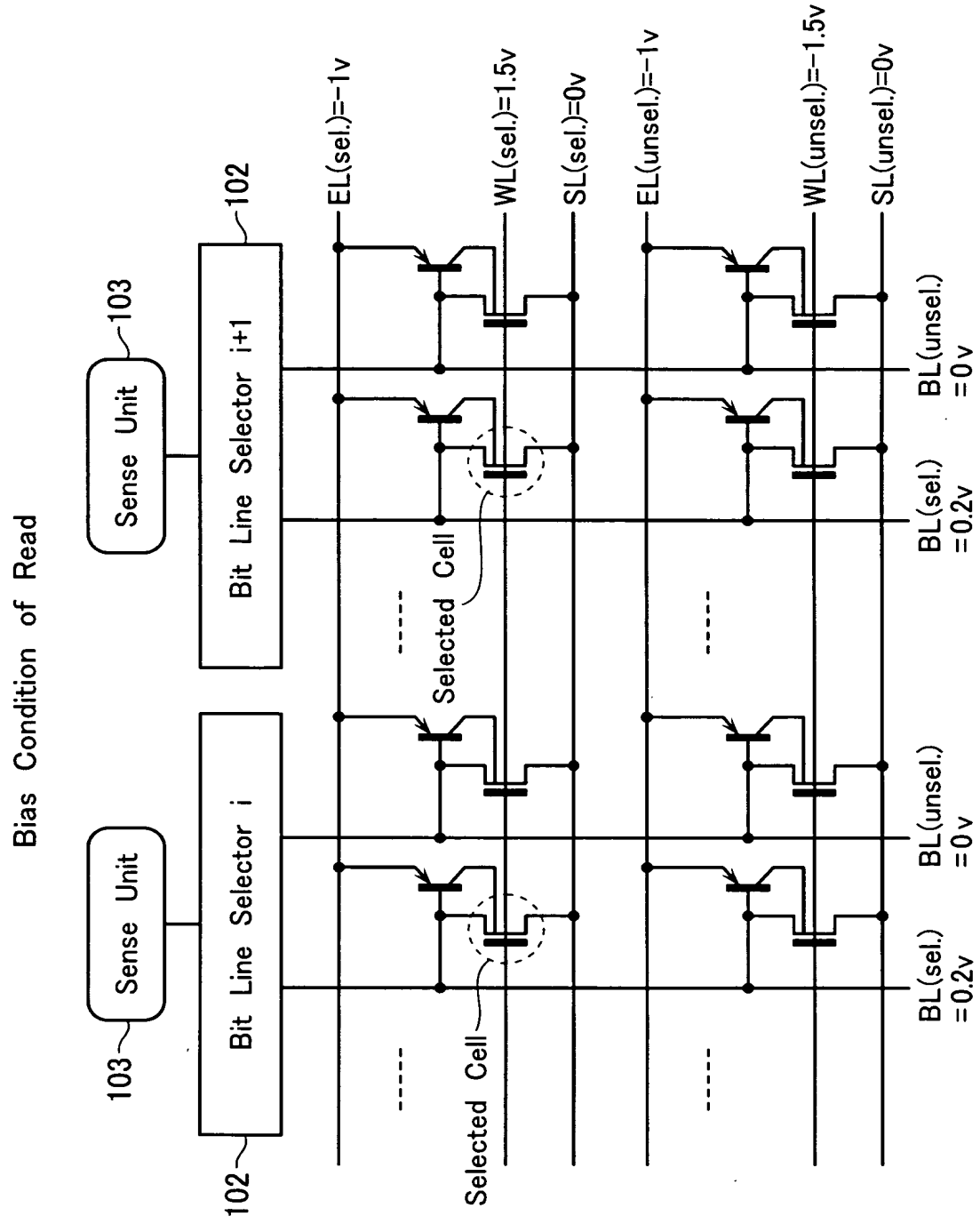


FIG. 14

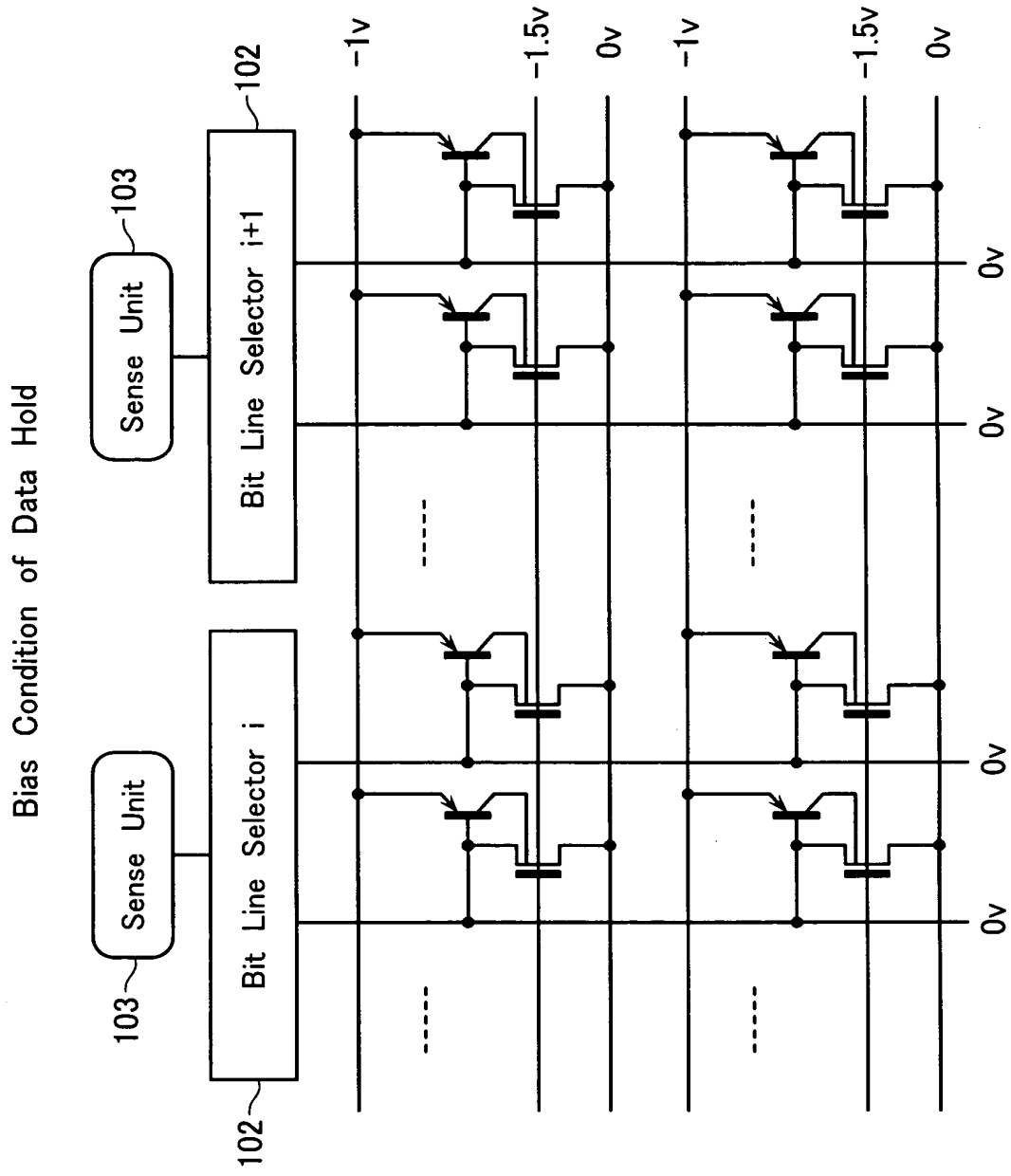


FIG. 15

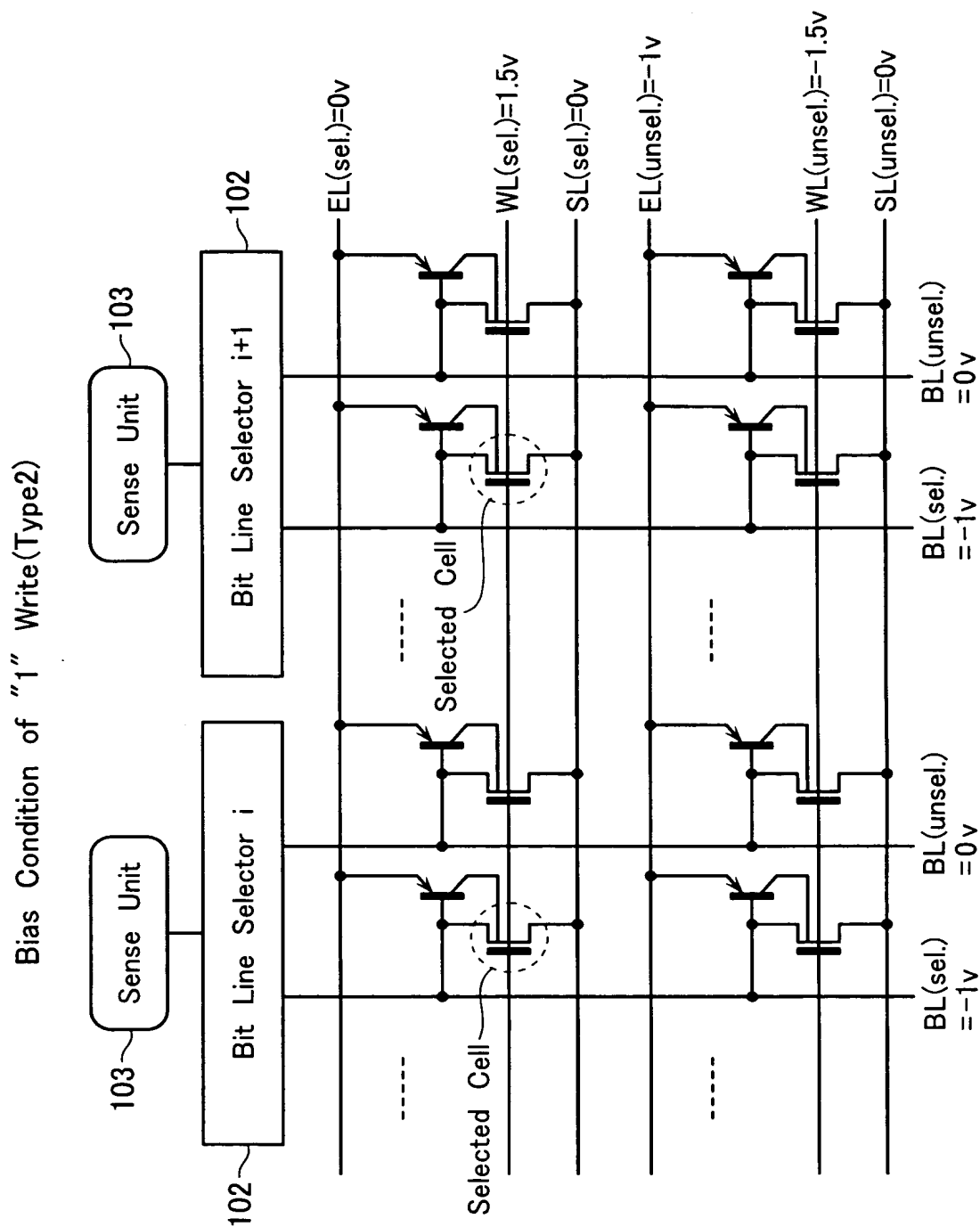
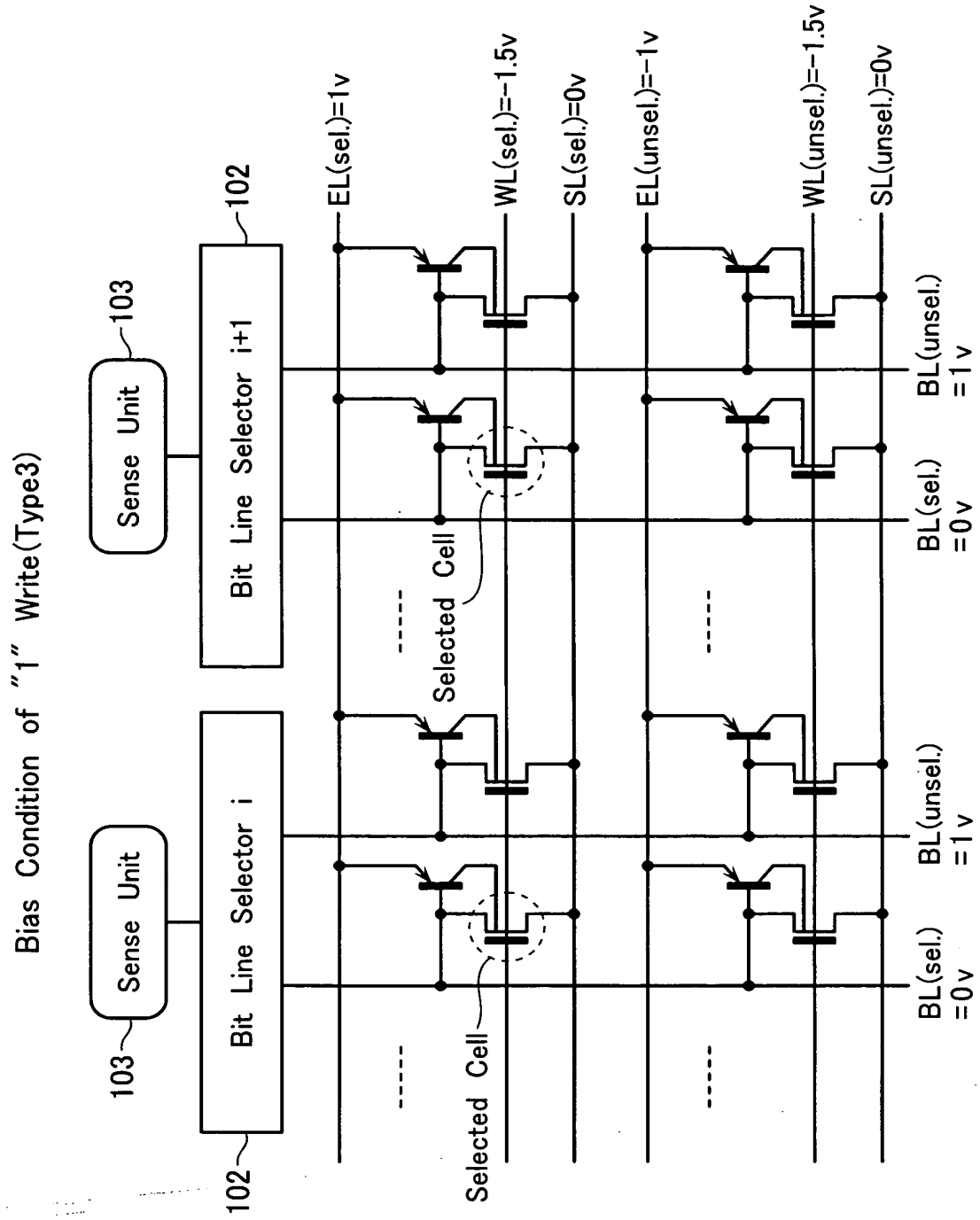


FIG. 16



- (1) $VELS \geq VBLS + V1$
 - (2) $VELS \leq VBLU + V0$
 - (3) $VELU \leq VBLS + V0$
- ($V1 > Vd0 \geq 0$)

FIG. 17

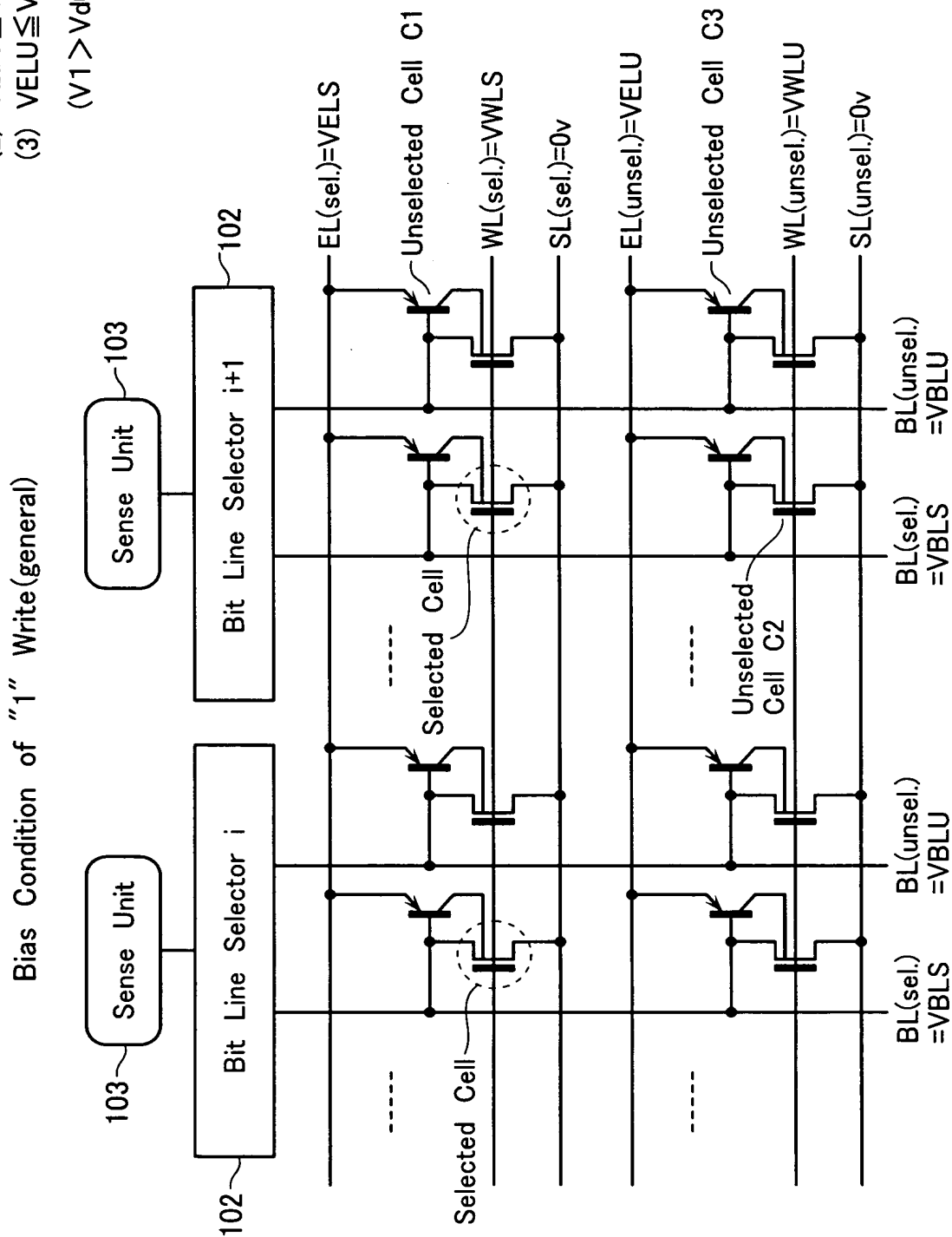


FIG. 18

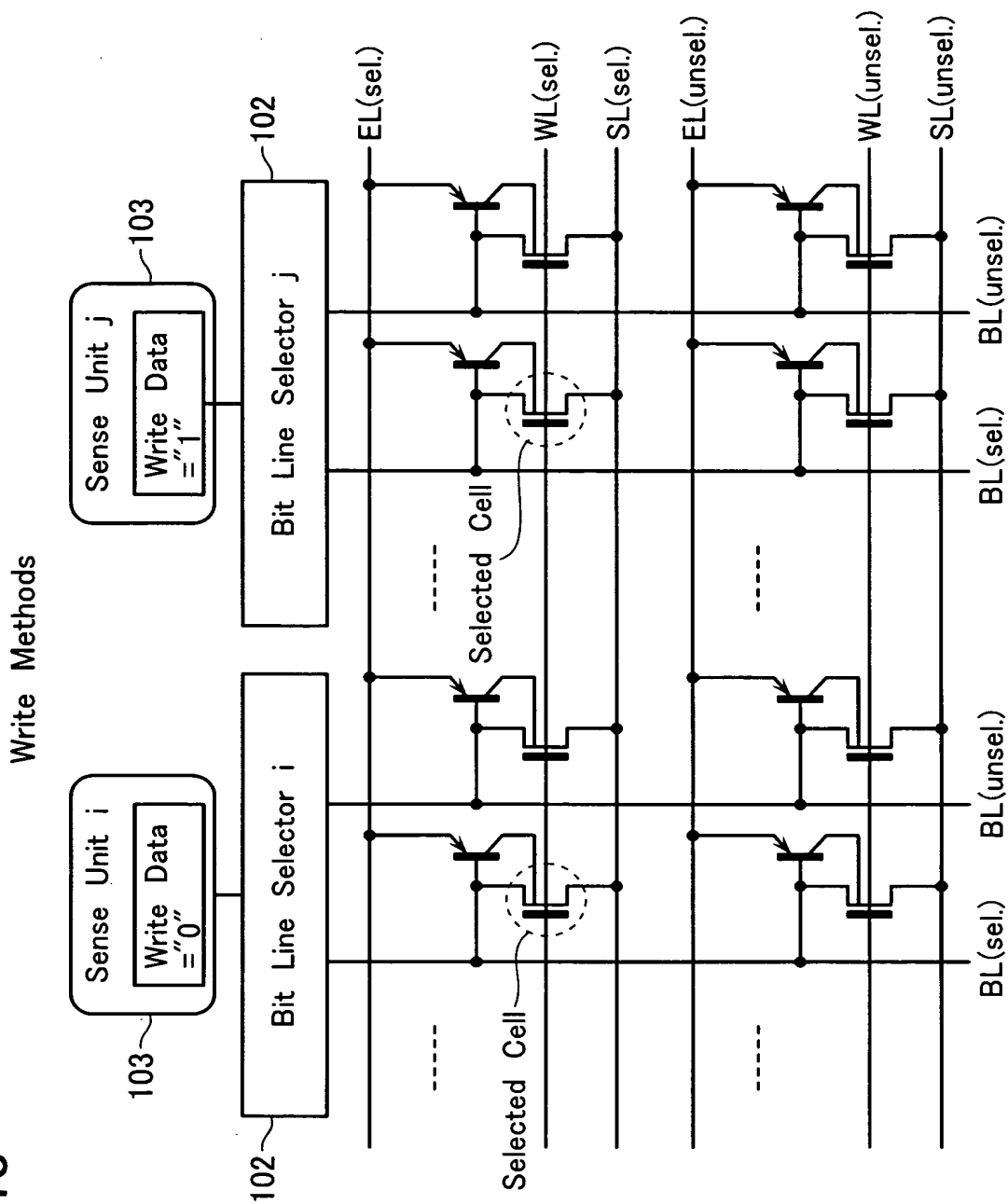


FIG. 19

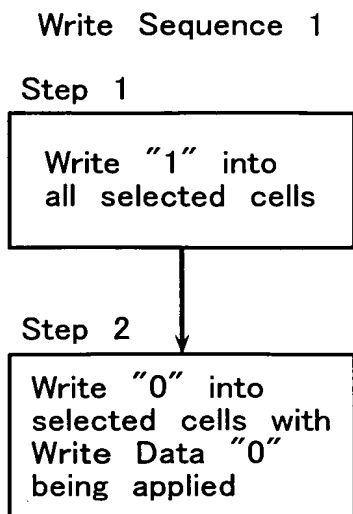


FIG. 20

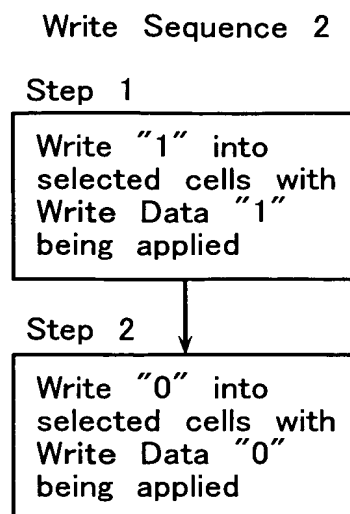


FIG. 21

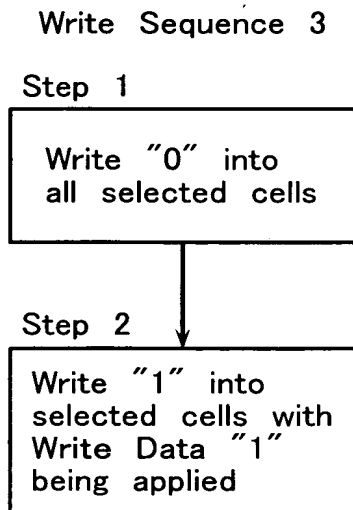


FIG. 22

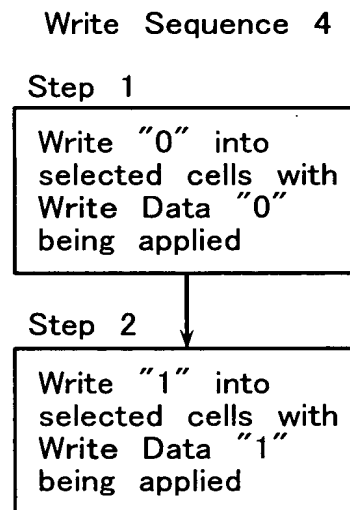


FIG. 23

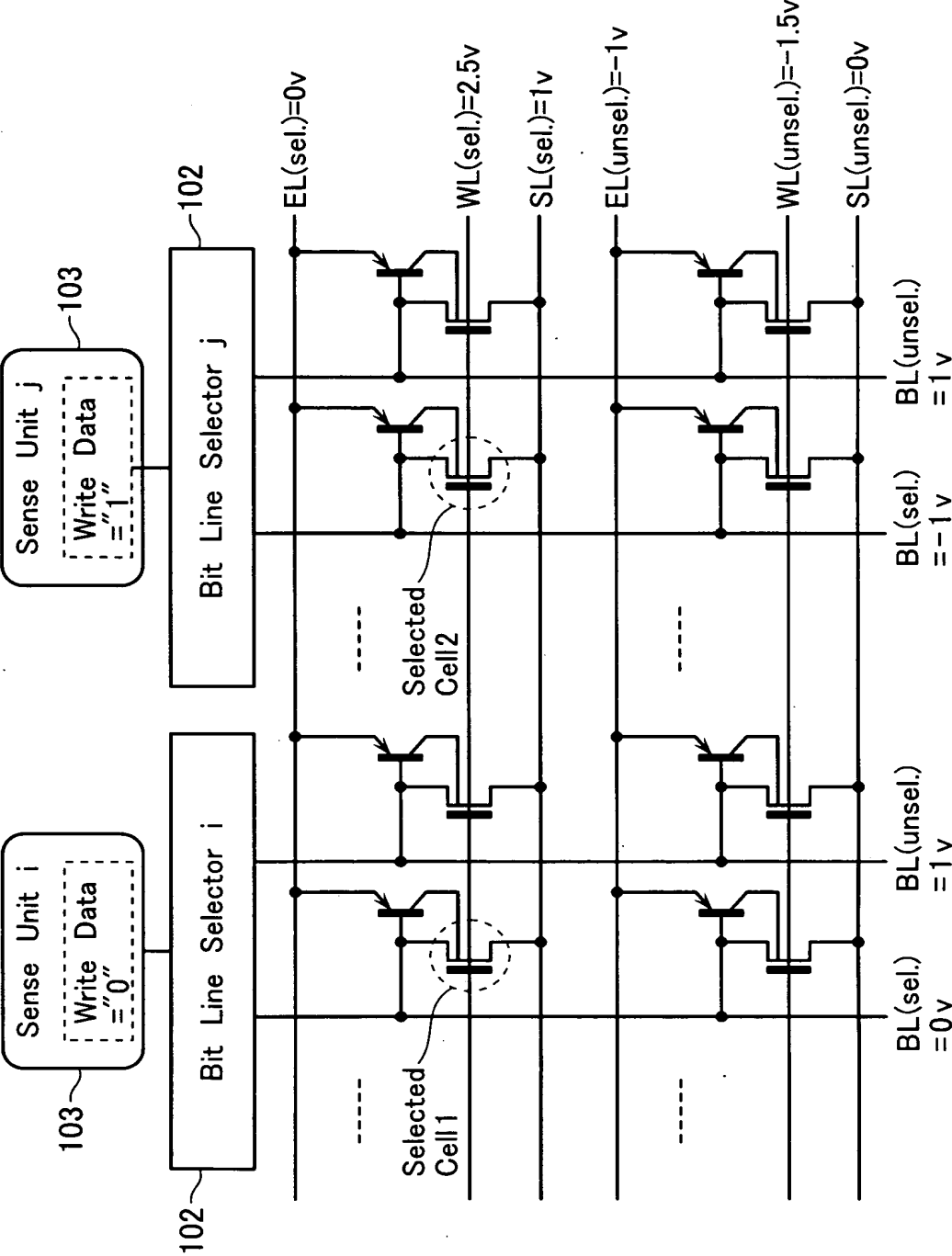


FIG. 24

Memory Cell Array

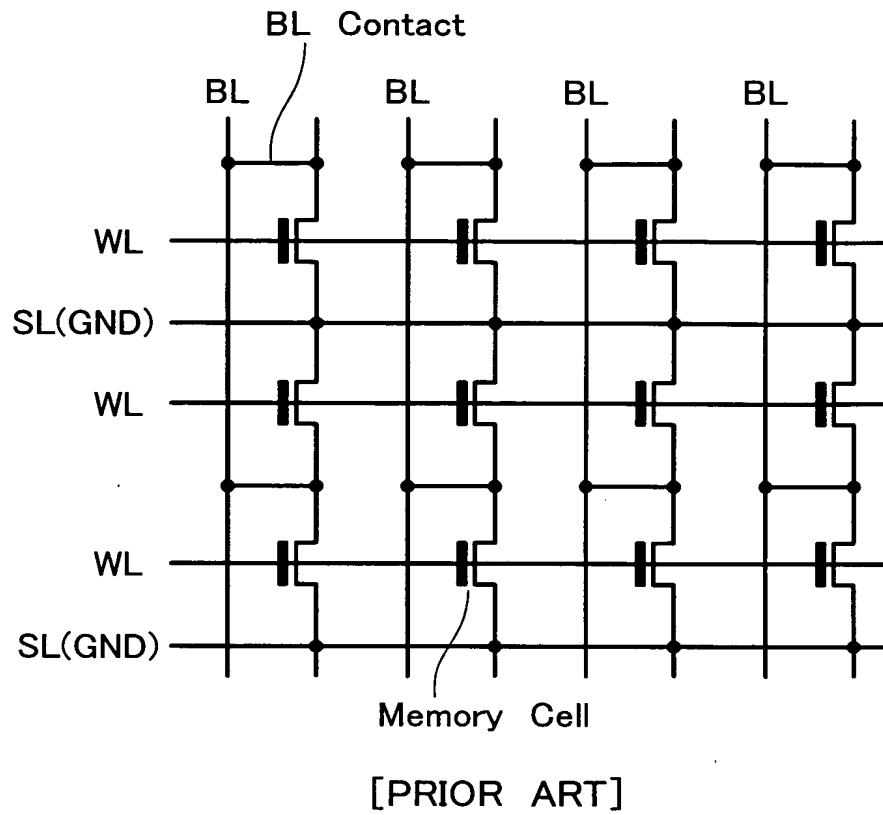


FIG. 25

"1" WRITE

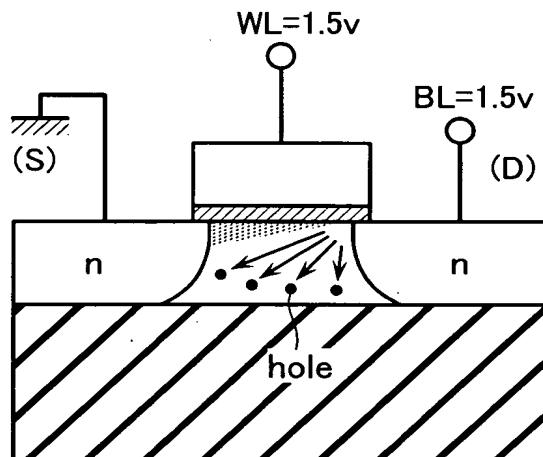
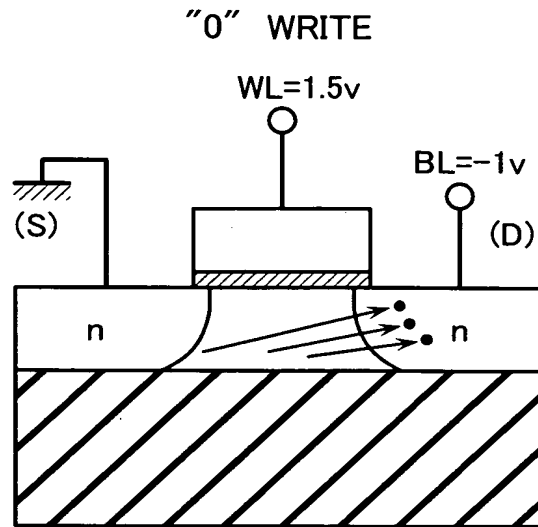
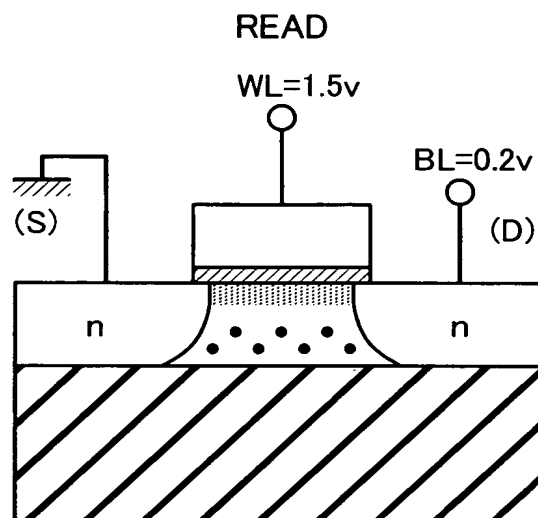


FIG. 26



[PRIOR ART]

FIG. 27



[PRIOR ART]

FIG. 28

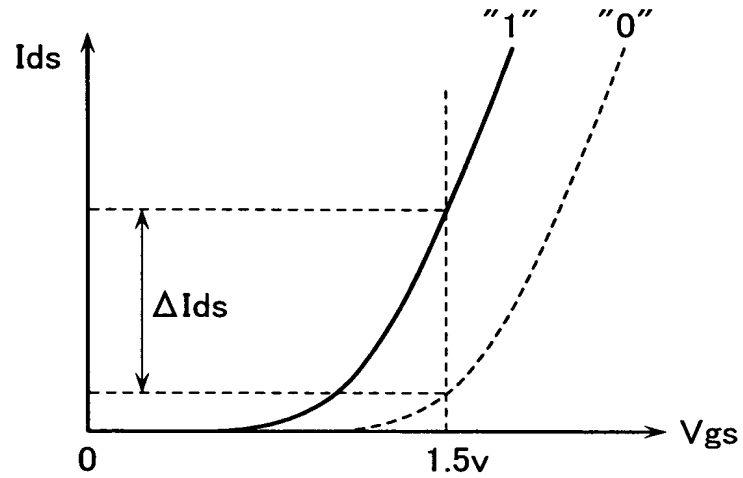
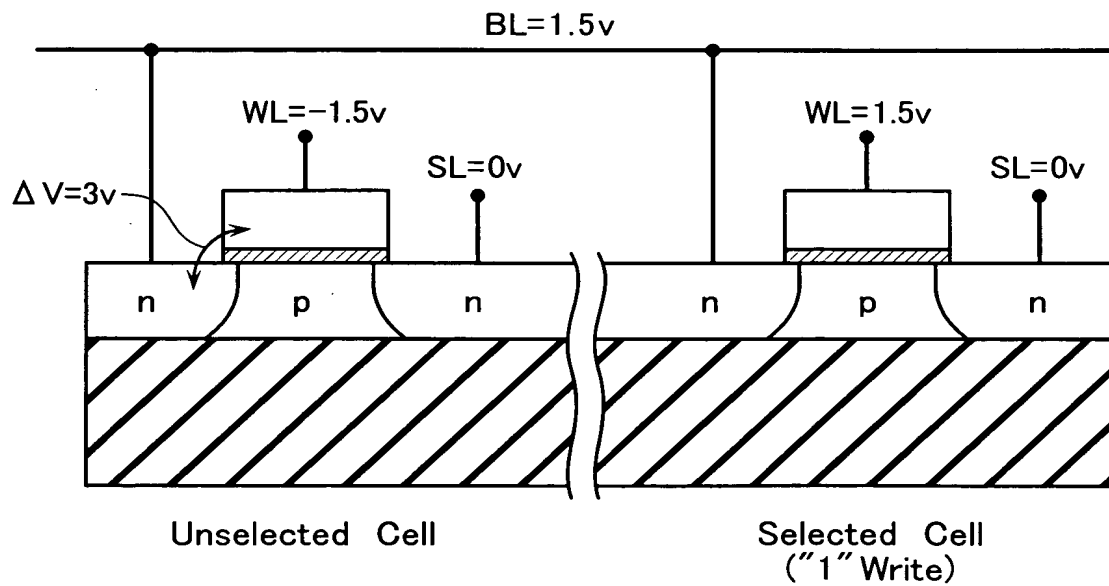


FIG. 29

Bias Condition of Unselected Cell



[PRIOR ART]